Digital Design Lab 5

Tara Moses

Section L001

October 27, 2015

tsmoses@uark.edu

**Abstract**

The purpose of this lab was to construct an adder/subtractor and to test the design of it using a simulation before implementing it on the FPGA board. An adder/sub was created and simulated using the Quartus II software.

**Introduction**

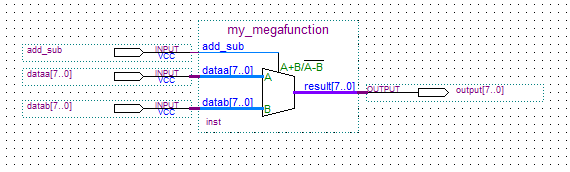
Quartus II is software that allows the user to create logic circuits and connect them to hardware. It works by letting the user drag and drop basic logic gates such as NOR, AND, OR, etc. The software offers various forms of these logic gates, each having a different number of inputs. After the logic circuit has been made, the user can rename each input (e.g. “switch 1”, “button 2”) and output (e.g. “LED”) to make the circuit easier to understand.

An adder/subtractor uses a multiplexer to add the two bus input sets if the add/sub input is equal to 1 and subtract the second bus input sets from the first if the add/sub input is equal to 0. Each bus input set is basically an array of integers, and the output of the adder/subtractor is another bus set.

This lab was designed to familiarize the student with using Quartus II to create a circuit and simulate it on the computer software before implementing it on the FPGA hardware. In this lab, an adder/sub circuit was designed in Quartus II and test inputs were added to it in waveform format. The circuit was tested by running a simulation in Quartus II. The circuit was expected to output the sum of the two inputs when the add/sub input equaled 1 and the difference of the second input minus the first if the add/sub input equaled 0.

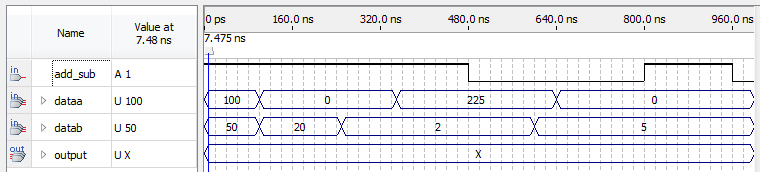
**Design and Implementation**

In Quartus II, a new schematic file was created and an adder/sub was added to it. Three inputs were added to it: two buses of integers to be added with and subtracted from each other, and a single input to decide whether the adder/sub would add or subtract the input buses. An output bus was added to the schematic to save the sums and differences. The inputs and outputs were renamed for readability. The finished schematic file is shown in Figure 1 below.



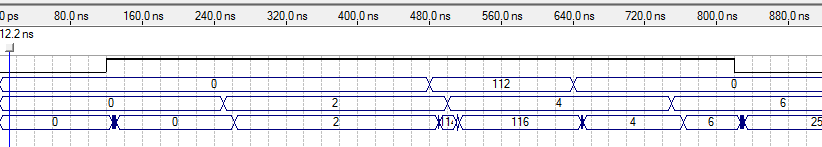
**Figure 1**: schematic diagram of adder/sub with 3 inputs and 1 output bus.

After the schematic was created and compiled, test cases were added to it by using a waveform diagram. The test cases are shown in Figure 2 below.



**Figure 2**: test cases for the circuit. From top to bottom: add/sub input (0 for subtraction, 1 for addition), first input bus, second input bus, and output bus (X).

Once the test cases were completed, the circuit was compiled again, and a simulation was run. The results of this simulation are shown in Figure 3 below.



**Figure 3**: simulation results for adder/sub circuit.

For every instance in which the add/sub input was 1, the values of the first and second input buses at that time were added together to form the value of the output bus at that time. For every instance in which the add/sub input was 0, the value of the second input bus at that time was subtracted from the value of the first input bus at that time. Every value in the output bus is correct except for the time range of 830 ns to 960 ns, in which case the output was supposed to be -6. The output is incorrect (it displays 251 instead) at these times because the adder/sub cannot account for integer overflow.

**Results**

The adder/subtractor successfully added and subtracted the given inputs for most cases. However, in cases where the absolute value of the actual sum or difference was greater than 256, overflow occurred and the calculated sum or difference was wrong. This is due to the fact that Quartus II used a 10-bit unsigned binary number for the adder/sub, and as a result any negative number was unable to be represented.

**Conclusion**

The lab was designed to give students a hands-on experience with simulating logic circuits pre-implementation on hardware. Using Quartus II and the FPGA board, a logic circuit was created to model an adder/sub. The adder/subtractor successfully added and subtracted inputs. One large source of error was the fact that the adder/subtractor, while working with binary signed integers, could not account for overflow. This resulted with the sum of two positive numbers being negative and vice versa. Overall, the project was successful. In the future, larger and more complex circuits that might be difficult to test on the FPGA board could be simulated on software to make it easier to verify. The lab took about an hour to complete.